REMARKS

Claims 1 – 38 remain in the application. Claims 1, 6, 10, 11, 14, 16, 18, 19, 24, 26, 31, 35, 36 and 38 stand rejected. Claims 2 – 9, 11 – 17, 19 – 30 and 32 – 37 are found to encompass patentable subject matter. Claims 1 – 5, 7 – 9, 12, 13, 15, 17, 20 – 30, 32 – 34 and 37 are objected to. Claims 1, 4, 6, 11 – 13, 18, 19, 22, 24, 28, 29, 31 and 36 are amended herein. The rejection is respectfully traversed.

Claims 1, 4, 22 and 26 have been objected to for formal reasons. Responsive thereto, claims 1, 4 and 22 are amended herein. Regarding the objection to claim 26, it is asserted that "locating said side drive point" lacks antecedent basis. However, claim 26 depends from claim 25, which recites "a side drive point." Accordingly, claim 25 provides antecedent basis for the objected to recitation of claim 26. Reconsideration and withdrawal of the objection to claims 1, 4, 22 and 26 is respectfully requested. No new matter has been added.

Amendments to claims 12, 13, 28 and 29 are formal in nature. No new matter has been added.

Claims 6, 11, 14, 16, 18, 19, 24, 26, 35 and 36 are rejected under 35 U.S.C. §112 as being indefinite. Partially responsive thereto, claims 6, 11, 18, 19, 24, 35 and 36 are amended herein. Although no specific allegation of indefiniteness is cited with respect to claim 26, it is believed that the above discussion of claim 26 addresses any issues of indefiniteness. No new matter has been added.

Regarding claims 11, 14, 16, 19 and 35, it is asserted that claims 11, 19 and 35 are indefinite because of the recitation of "level converter fanin cones;" that claims 16 and 19 are indefinite for reciting "first voltage level buffer;" and that claims 14 and 19 are indefinite because of the recitation of "second voltage level circuit elements" and that "first voltage level circuit elements" lacks antecedent basis. The MPEP provides in pertinent part that

> 2173.02 Clarity and Precision [R-1] The examiner's focus during examination of claims for compliance with the requirement for

> definiteness of 35 U.S.C. 112, second paragraph, is whether the claim meets the threshold requirements of clarity and precision, not whether more suitable language or modes of expression are available. When the examiner is satisfied that patentable subject matter is disclosed, and it is apparent to the examiner that the claims are directed to such patentable subject matter, he or she should allow claims which define the patentable subject matter with a reasonable degree of particularity and distinctness. Some latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the examiner might desire. Examiners are encouraged to suggest claim language to applicants to improve the clarity or precision of the language used, but **should not reject claims or insist on their own preferences** if other modes of expression selected by applicants satisfy the statutory requirement.
> (emphasis added.)

Regarding "level converter fanin cones," a quick keyword search on "fanin cone" on the Internet (e.g., using the Yahoo! search engine) produces 124 hits. A similar search on the PTO database produces 24 hits for issued patents and 23 hits for published applications. Thus, it is apparent that "fanin cone" has a wellknown meaning in the art. Further, "fanin cones" are specifically described in the present application at page 13, line 27 – page 14, line 1 with reference to Figures 7A – B and 8. Thus, "level converter fanin cones" are "fanin cones" for the level converters and would be clearly understood by a person of skill in the art.

Regarding "first [and second] voltage level circuit elements," claim 19, for example, is directed to a "method of optimizing level converter placement in a multi supply integrated circuit design" at lines 1 – 2. *See also*, claim 1 (as amended), lines 1 – 2 and claim 31, line 2. Further, each of claim 1 (lines 5 – 6), claim 19 (lines 6 – 7) and claim 31 (lines 8 – 9), recites "a **first voltage** net delay to said level converter, through said level converter and a **second voltage** net delay" (emphasis added). Thus, clearly "first voltage level circuit elements" are circuit elements connected to first voltage nets and "second voltage level circuit elements" are circuit elements connected to second voltage nets of the multi supply design. Similarly, with respect to claim 16, claim 6 recites "first voltage level buffer and level converter pairs," which clearly refers to

instances of a level converter paired with a "first voltage level buffer," i.e., a circuit element (a buffer) connected to first voltage nets. Accordingly, it is believed that neither the recitation of "level converter fanin cones" nor of "first [and second] voltage level circuit elements [or buffers]," makes any of claims 11, 14, 16, 19 or 35 indefinite. Reconsideration and withdrawal of the rejection of claims 6, 11, 14, 16, 18, 19, 24, 26, 35 and 36 under 35 U.S.C. §112 and allowance of claims 19 – 30 is respectfully requested.

Claims 1, 10, 18, 31 and 38 are rejected under 35 U.S.C. §102(b) over each of "On Gate Level Power Optimization Using Dual-Supply Voltages" to Chen et al. and "A Low-power Design Method Using Multiple Supply Voltages" to Igarashi et al., and under 35 U.S.C. §102(a) over "Multiple Vdd Scheduling/Allocation for Partitioned Floorplan" to Kung et al. The rejection is respectfully traversed.

The applicants note at the outset that Kang et al. published less than two months before the filing date of the present application. Thus, the applicants can, if necessary, show an invention date prior to the Kang et al. publication date. However such a showing is not believed necessary for the reasons set forth below.

Regarding claim 1 (and analogously, claim 31), it is asserted that "selectively placing each level converter at a minimum power point to minimize net power and transitional delay, transitional delay being a first voltage net delay to said level converter, through said level converter and a second voltage net delay from said level converter" is taught by: section IV of Chen et al.; sections 3 and 5 of Igarashi et al.; and, the Abstract and section 2 of Kung et al. Each of these references teaches determining a *figurative* point for the particular multi supply design, where one balances the power savings realized from using lower voltage gates with the additional delay incurred as a result of using the lower voltage gates. Thus, Chen et al. indicates that "[t]he estimate given by (6) is *optimal* in the sense that any deviation from it will either increase power consumption or violate the timing constraints." (Italics original.) Igarashi et al. notes that "it is difficult to keep the circuit performance while reducing the supply voltage of the circuit." Last sentence of the first paragraph of Igarashi et al. section 1. Igarashi et al. section 3 vaguely describes locating level converters between low voltage and high

voltage circuits; and section 5 discusses placing circuits to minimize wire length but fails to discuss placing level converters at all. Igarashi et al. section 6 discusses only locating the level converters in "a VDDH cell row to supply the VDDH." Third paragraph, fourth sentence. Similarly, Kang et al. describes a partitioning algorithm to assign circuits to high or low voltage cells. *See, e.g.*, Kang et al. Figure 4, the next to last clock: "Return a schedule with minimum energy for [Type] that satisfy the resource constraints." Once such an assignment is complete, level converters may be inserted, but Kang et al. is silent on the location of any such inserted level converter.

The present application specifically provides that "the optimum level converter 200 placement is a location to minimize the total wire length; and also, allocates the largest portion of that wire length to the low supply voltage side (i.e., driven by the V_{ddl} driver 190) to minimize switching power, i.e., power expended driving the wire load." Page 12, lines 10 – 13. The specification describes a number of examples for determining the optimum level converter placement. In the specific "example of Figure 6C the level converter 200 is located a minimum power point at (X_{min}, Y_{min}), ..." *Id*, lines 13 – 14. None of the references of record teaches or suggests identifying a literal minimum power point to optimize level converter placement. Therefore, neither Chen et al., Igarashi et al. or Kang et al. teaches or suggests the present invention as recited in either of claims 1 and 31.

Furthermore, since dependent claims include all of the differences with the prior art as the claims from which they depend, neither Chen et al., Igarashi et al. or Kang et al. teaches or suggests the present invention as recited in claims 10, 18 or 38, which depend from claims 1 and 31, respectively. Reconsideration and withdrawal of the rejection of claims 1, 10, 18, 31 and 38 under 35 U.S.C. §102(b) over each of Chen et al. and Igarashi et al. and under 35 U.S.C. §102(a) over Kang et al. is respectfully requested.

The applicants have reviewed the references cited but not relied upon and find them to be no more relevant than the references upon which the rejection is based.

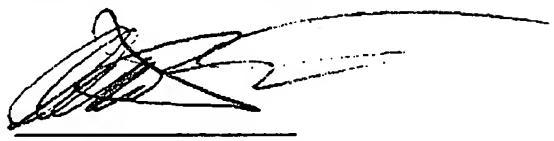
The applicants thank the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance, both for the

amendment to the claims and for the reasons set forth above, the applicants respectfully request that the reconsider and withdraw the objection to claims 1 – 5, 7 – 9, 12, 13, 15, 17, 20 – 30, 32 – 34 and 37, the rejection of claims 6, 11, 14, 16, 18, 19, 24, 26, 35 and 36 under 35 U.S.C. §112 and the rejection of claims 1, 10, 18, 31 and 38 under 35 U.S.C. §§102(a) and (b) and allow the application to issue.

Should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-0510 and advise us accordingly.

Respectfully Submitted,



February 23, 2006
(Date)

Charles W. Peterson, Jr.
Registration No. 34,406

Customer No. 33233
Law Office of Charles W. Peterson, Jr.
11703 Bowman Green Dr,
Suite 100
Reston, VA 20190
Telephone: (703) 481-0532
Facsimile: (703) 481-0585